Appl. No. 09/692,420
Amdt. dated Oct. 5, 2005
Reply to Office action of May 5, 2005

Listing of the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Original) A filter circuit, comprising:

a plurality of cascaded filters; and

a bypass circuit coupled across one of the cascaded filters.

2. (Original) The filter circuit of claim 1 wherein the bypass circuit comprises a switch.

3. (Previously Presented) The filter circuit of claim 1 further comprising a plurality of bypass circuits including the bypass circuit, the bypass circuit each being coupled across a different one of the cascaded filters.

4. (Original) The filter circuit of claim 3 wherein each of the bypass circuits are adapted for individual control.

5. (Original) The filter circuit of claim 3 wherein the bypass circuits each comprises a switch.

6. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises a biquad filter.

7. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises a complex filter.

8. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises a differential filter.

9. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises a pole and a zero.

10. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises a complex filter with a pole and a zero.

11. (Original) The filter circuit of claim 1 wherein the cascaded filters each comprises first and second amplifiers each having a feedback loop comprising a feedback resistor and feedback capacitor coupled in parallel.

12. (Original) The filter circuit of claim 11 wherein at least one of the feedback resistors is programmable.

13. (Original) The filter circuit of claim 12 wherein said at least one programmable feedback resistor comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

14. (Original) The filter circuit of claim 11 wherein at least one of the feedback capacitors is programmable.

15. (Original) The filter circuit of claim 14 wherein said at least one programmable feedback capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

16. (Original) The filter circuit of claim 11 wherein the cascaded filters each comprises a first cross coupled resistor coupled between an output of the first amplifier and an input of the second amplifier, and a second cross coupled resistor coupled between an output of the second amplifier and an input of the first amplifier.

17. (Original) The filter circuit of claim 16 wherein the cascaded filters each comprises a first input resistor coupled to the input of the first amplifier, and a second input resistor coupled to the input of the second amplifier.

18. (Original) The filter circuit of claim 16 wherein the cascaded filters each comprises an input capacitor having one end coupled to the first input resistor and a second end coupled to the second input resistor.

19. (Original) The filter circuit of claim 18 wherein at least one of the capacitors is programmable.

20. (Original) The filter circuit of claim 19 wherein said at least one programmable capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

21. (Original) The filter circuit of claim 18 wherein at least one the resistor is programmable.

22. (Original) The filter circuit of claim 21 wherein said at least one programmable resistors comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

23. (Original) A filter circuit, comprising:
a plurality of cascaded filters; and
bypass means for bypassing at least one of the cascaded filters,

24. (Original) The filter circuit of claim 23 wherein the bypass means comprises a switch coupled across one of the cascaded filters.

25. (Original) The filter circuit of claim 23 wherein the bypass means comprises a plurality of switches each being coupled across a different one of the cascaded filters.

26. (Original) The filter circuit of claim 23 wherein the switches each comprises means for being individually controlled.

27. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises a biquad filter.

28. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises a complex filter.

29. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises means for generating a pole and zero.

30. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises a complex filter, the complex filters each comprising means for generating a pole and zero.

31. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises first and second amplifiers each having a feedback loop comprising a feedback resistor and feedback capacitor coupled in parallel.

32. (Original) The filter circuit of claim 31 wherein at least one of the feedback resistors comprises means for being programmed to one of a plurality of resistive values.

33. (Original) The filter circuit of claim 32 wherein the means for being programmed comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

34. (Original) The filter circuit of claim 31 wherein at least one of the feedback capacitors comprises means for being programmed to one of a plurality of capacitive values.

35. (Original) The filter circuit of claim 34 wherein the means for being programmed comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

36. (Original) The filter circuit of claim 31 wherein the cascaded filters each comprises a first cross coupled resistor coupled between an output of the first amplifier and an input of the second amplifier, and a second cross coupled resistor coupled between an output of the second amplifier and an input of the first amplifier.

37. (Original) The filter circuit of claim 36 wherein the cascaded filters each comprises a first input resistor coupled to the input of the first amplifier, and a second input resistor coupled to the input of the second amplifier.

38. (Original) The filter circuit of claim 37 wherein the cascaded filters each comprises an input capacitor having one end coupled to the first input resistor and a second end coupled to the second input resistor.

39. (Original) The filter circuit of claim 38 wherein at least one of the capacitors comprises means for being programmed to one of a plurality of capacitive values.

40. (Original) The filter circuit of claim 39 wherein the means for being programmed comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

41. (Original) The filter circuit of claim 38 wherein at least one the resistor comprises means for being programmed to one of a plurality of resistive values.

42. (Original) The filter circuit of claim 41 wherein the means for being programmed comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

43. (Original) The filter circuit of claim 23 wherein the cascaded filters each comprises a differential filter.

44. (Previously Presented) A filter circuit, comprising:
a biquad filter; and
a polyphase filter coupled to the biquad filter.

45. (Previously Presented) The filter circuit of claim 44 further comprising a plurality of biquad filters including the biquad filter, and a plurality of polyphase filters including the polyphase filter, the biquad filters being intertwined with the polyphase filters.

46. (Previously Presented) The filter circuit of claim 45 further comprising a plurality of bypass circuits each being coupled across a different one of the biquad filters.

47. (Original) The filter circuit of claim 46 wherein each of the bypass circuits are adapted for individual control.

48. (Original) The filter circuit of claim 46 wherein the bypass circuits each comprises a switch.

49. (Original) The filter circuit of claim 44 wherein the filters each comprises a differential filter.

50. (Original) The filter circuit of claim 44 wherein the biquad filters each comprises first and second amplifiers each having a feedback loop comprising a feedback resistor and feedback capacitor coupled in parallel.

51. (Original) The filter circuit of claim 50 wherein at least one of the feedback resistors is programmable.

52. (Original) The filter circuit of claim 51 wherein said at least one programmable feedback resistor comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

53. (Original) The filter circuit of claim 50 wherein at least one of the feedback capacitors is programmable.

54. (Original) The filter circuit of claim 53 wherein said at least one programmable feedback capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

55. (Original) The filter circuit of claim 50 wherein the biquad filters each comprises a first cross coupled resistor coupled between an output of the first amplifier and an input of the second amplifier, and a second cross coupled resistor coupled between an output of the second amplifier and an input of the first amplifier.

56. (Original) The filter circuit of claim 55 wherein the biquad filters each comprises a first input resistor coupled to the input of the first amplifier, and a second input resistor coupled to the input of the second amplifier.

57. (Original) The filter circuit of claim 56 wherein the biquad filters each comprises an input capacitor having one end coupled to the first input resistor and a second end coupled to the second input resistor.

58. (Original) The filter circuit of claim 57 wherein at least one of the capacitors is programmable.

59. (Original) The filter circuit of claim 58 wherein said at least one programmable capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

60. (Original) The filter circuit of claim 57 wherein at least one the resistor is programmable.

61. (Original) The filter circuit of claim 60 wherein said at least one programmable resistors comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

62. (Previously Presented) A complex differential filter, comprising:

first and second differential amplifiers each having a differential input and a differential output;

a first input resistor coupled to a first one of the differential inputs of the first differential amplifier;

a second input resistor coupled to a second one of the differential inputs of the first differential amplifier;

a third input resistor coupled to a first one of the differential inputs of the second differential amplifier;

a fourth input resistor coupled to a second one of the differential inputs of the second differential amplifier;

a first input capacitor having one end coupled to the first input resistor and another end coupled to the third input resistor;

a second input capacitor having one end coupled to the second input resistor and another end coupled to the fourth input resistor;

a third input capacitor having one end coupled to the third input resistor and another end coupled to the second input resistor; and

a fourth input capacitor having one end coupled to the fourth input resistor and another end coupled to the first input resistor.

63. (Original) The complex differential filter of claim 62 wherein at least one of the input resistors is programmable.

64. (Original) The complex differential filter of claim 63 wherein said at least one programmable input resistor comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

65. (Original) The complex differential filter of claim 62 wherein at least one of the input capacitors is programmable.

66. (Original) The complex differential filter of claim 65 wherein said at least one programmable input capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

67. (Original) The complex differential filter of claim 62 wherein the first and second differential amplifiers each comprises a feedback loop comprising a feedback resistor and feedback capacitor coupled in parallel.

68. (Original) The complex differential filter of claim 62 wherein the first differential amplifier comprises a first feedback loop coupled between a first one of its differential outputs and the first one of its differential inputs, and a second feedback loop coupled between a second

one of its differential outputs and the second one of its differential inputs, the feedback loops each comprising a feedback resistor and feedback capacitor coupled in parallel.

69. (Original) The complex differential filter of claim 68 wherein the second differential amplifier comprises a third feedback loop coupled between a first one of its differential outputs and the first one of its differential inputs, and a second feedback loop coupled between a second one of its differential outputs and the second one of its differential inputs, the third and fourth feedback loops each comprising a feedback resistor and feedback capacitor coupled in parallel.

70. (Original) The complex differential filter of claim 69 further comprising a first cross coupled resistor coupled between the first one of the differential outputs of the first differential amplifier and the second one of the differential inputs of the second differential amplifier, a second cross coupled resistor coupled between a second one of the differential outputs of the first differential amplifier and the first one of the differential inputs of the second differential amplifier, a third cross coupled resistor coupled between the first one of the differential outputs of the second differential amplifier and the first one of the differential inputs of the first differential amplifier, and a fourth cross coupled resistor coupled between a second one of the differential outputs of the second differential amplifier and the second one of the differential inputs of the first differential amplifier.

71. (Original) The complex differential filter of claim 70 wherein at least one of the capacitors is programmable.

72. (Original) The complex differential filter of claim 71 wherein said at least one programmable capacitor comprises a plurality of capacitors coupled in parallel, said plurality of capacitors each having a switch coupled thereacross.

73. (Original) The complex differential filter of claim 70 wherein at least one the resistor is programmable.

74. (Original) The complex filter of claim 73 wherein said at least one programmable resistors comprises a plurality of resistors coupled in series, said plurality of resistors each having a switch coupled thereacross.

75. (Original) A method of complex filtering to extract a signal in a frequency spectrum comprising a plurality of channels, comprising:

selecting one of the channels having the signal;

rejecting an image of the signal in the selected channel; and

applying gain to the signal, the applied gain being programmable.

76. (Original) The method of claim 75 wherein the channel selection comprises tuning a center frequency of the channel.

77. (Original) The method of claim 76 wherein the channel selection further comprises tuning a bandwidth of the channel.

78. (Original) The method of claim 75 further comprising introducing a zero to filter a frequency in the selected channel different from a frequency of the signal.

79. (Original) The method of claim 75 further comprising introducing a plurality of zeros each filtering a different frequency in the selected channel, the filtered frequencies each being different from a frequency of the signal.

80. (Original) The method of claim 79 further wherein the introducing of the zeros comprises programming the number of the zeros introduced.

81. (Original) The method of claim 75 wherein the channel selection further comprises programming an order of complex filtering.